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Toward High-Speed and Energy-Efficient Computing: A WDM-Based Scalable On-Chip Silicon Integrated Optical Comparator

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Integrated photonics has shown extraordinary potential in optical computing. Various optical computing modules have been investigated, among which the digital comparator is a significant element for any arithmetic logic unit. In this study, an architecture of a wavelength-division-multiplexing-based (WDM-based) electronic–photonic digital comparator is proposed, which can perform high-bit comparisons for fixed-point or floating-point binary inputs. A silicon photonics-based 2-bit comparator operating at 20 Gb s^{-1} at a 1.55 μm wavelength is experimentally demonstrated. A detailed performance analysis reveals that this architecture outperforms the current transistor-based electronic comparators in terms of both computational speed and power efficiency.

1. Introduction

The past decades have witnessed the stagnation of the clock rate of electronic central processing units (CPUs) because of the overwhelming heat dissipation, and the power consumption per bit of modern microprocessors is almost close to saturation.[1,2] Consequently, the continuation of Moore's law has become problematic. Integrated photonics has the potential to overcome these limitations and replace transistor-based electrical circuits to process information owing to the key features of light, which are low latency and a high bandwidth. Using photons as the signal carrier provides us with a wavelength-division multiplexing scheme that is exclusively available for integrated photonics.[3,4] Moreover, the current fabrication technologies allow photonic components and transistors to be integrated on the same chip, paving the way for inter- and intra-chip communications [5,6] between electronic modules and photonic modules to realize complex computing functions.[7,8] Numerous concepts for realizing hardware implementations for optical computing have been proposed recently to envision feasible approaches.[9–13]

Researchers have paid significant attention to optical digital circuits for computing because of the advantages of digital computing such as high noise tolerance and energy efficiency, which have been proven by decades of successful practical experience of very-large-scale integration (VLSI). Abundant passive and active building blocks for digital optical computing and interconnects on integrated photonic platforms have been experimentally demonstrated and have been provided by foundries, such as electro-optic (EO) switches and modulators.[14–17] Digital logic gates [18–21] and basic digital logic modules including but not limited to adders,[22–24] comparators,[25] encoders,[12] and decoders[26] have been investigated in previous studies. Furthermore, logic synthesis specified for photonic circuits has been proposed for designing more complicated computing modules with a high bit size.[27,28]

Although numerous optical digital computing modules have been investigated, several unique features of photons have not been completely utilized in photonic integrated circuit design. For example, owing to the properties of bosons, photons with different wavelengths and other properties can independently propagate in the same space, which is promising for scaling down the chip size and the number of active components in photonic chips.[27] Previous studies have revealed that the number of EO logic gates can be reduced by using WDM to construct a carry-select electronic–photonic full adder.[24] The idea of utilizing these unique features of photons for scaling and performance optimization in photonic arithmetic unit designs is extended and improved in this study, where multiple wavelengths can implement different logic functions to realize comparison, an essential functional unit in modern microprocessors.

Furthermore, most proposed optical computing modules require the inputs to be unsigned, fixed-point numbers.[26,29] In

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real scenarios, the formats of the inputs can be signed or unsigned, fixed-point, or floating-point. The combinational logic circuits must be modified to obtain the correct computing results accordingly. In this study, we present the first photonic version of a digital comparator that can process signed or floating-point binary inputs.

A digital comparator is a fundamental arithmetic component in microprocessors, and it is also useful for image and signal processing.[30] Different structures have been proposed to improve the speed and power consumption of transistor-based electronic comparators, whereas the operating speed has been stagnated at up to 4 GHz.[31,32] Some studies have focused on designing optical comparators based on all-optical devices; however, the performance, as well as the bit size of their designs, is restricted by the difficulties of large-scale integration (i.e., 64-bit and above) of all-optical logic gates.[33,34] In the context of all-optical activation, strong pump light is required to trigger nonlinear effects, leading to tremendous power dissipation, which defeats the purpose. Direct-logic-based optical comparators have also been reported in literature, which use add-drop microresonator modulators as EO logic gates.[25,35] However, only designs of single-bit comparators are presented, and their schemes cannot be extended to design comparators with higher bits, such as 64 or 128 bits, which are required in current computing and communication applications. A simple example is the IPV6 (Internet Protocol version 6).[36] Although the architecture of an N-bit optical comparator is discussed in some studies,[26] the number of output ports is considerably high, which can dramatically increase the complexity if the comparison results are associated with other computing modules. Finally, all optical comparators mentioned above only support unsigned fixed-point comparisons. Thus, they will fail to compare two signed binary inputs, and they cannot be deployed in floating-point units.

In this study, we have devised a novel scheme to realize an N-bit wavelength-division-multiplexing-based (WDM-based) electronic–photonic digital comparator for high-speed and energy-efficient computation. We begin with the theoretical projection and implementation of the basic structure of the WDM-based electronic–photonic comparator (EPCMP), in which two wavelengths are used to represent two logic functions. A 2-bit EPCMP operating at 20 GHz was experimentally demonstrated. We also proposed the general architecture of a scalable EPCMP for fixed-point/floating-point binary number comparison, which exploits the advantages of electronics and photonics such as parallel computing and WDM. A detailed performance analysis of our EPCMP is provided, indicating that our architecture can run at tens of gigahertz while consuming much less power than state-of-the-art electronic comparators. Methods to optimize the performance of the EPCMP and to scale down the circuit size are also presented.

2. Architecture

A digital comparator compares and determines whether one binary number is greater, equal, or less than another. It has three primary outputs $A > B$, $A = B$, $A < B$, ($A = a_n a_{n-1} \dots a_2 a_1$, and $B = b_n b_{n-1} \dots b_2 b_1$), which can be determined using a subtractor and an equality comparator.

Table 1. Logic truth table for a digital comparator.

C	Z	Result
0	1	$A = B$
0	0	$A > B$
1	0	$A < B$

The subtractor determines the larger of the two binary numbers by computing $B - A - 1 = B + \overline{A}$. If there is a carry signal at the output, $A < B$; otherwise, $A \geq B$. A subtractor can be treated as a special full adder, the expression of which can be summarized as follows

$$C_k = (a_k \otimes b_k) \cdot C_{k-1} + \overline{a_k} \cdot b_k = p_k \cdot C_{k-1} + g_k \tag{1}$$

where $C_0 = 0$, $p_k = \overline{a_k} \oplus b_k = a_k \otimes b_k$ (propagate), and $g_k = \overline{a_k} \cdot b_k$(generate). "⊗" denotes the XNOR operation (The output is 1 if the logics of a_k and b_k are the same; otherwise, the output is 0.), whereas "·" denotes the AND operation in digital computing. The final carry signal from the last bit $C = C_n$ can be realized with any adder architecture, which has been investigated and optimized for the past decades. **Figure 1**a shows a schematic diagram of an n-bit comparator based on an n-bit ripple carry adder.

The equality comparator determines if $A = B$, which can be performed simply with XNOR gates and an all-ones detector (AOD). The output Z for the equality comparator can be written as follows

$$Z = (a_1 \otimes b_1) \cdot (a_2 \otimes b_2) \cdot \dots (a_n \otimes b_n) = p_1 p_2 \dots p_n \tag{2}$$

The final comparison result can then be determined using C and Z, as shown in **Table 1**. The detailed meanings of all logic signals are provided in Table S1 in the Supporting Information.

Figure 1b shows the general architecture of an EPCMP, where the critical path of the comparator architecture is replaced by an optical route because light has one to two orders of magnitude less latency per gate than the transistors. Light beams with different wavelengths can pass through the same structure independently to implement and convey C and Z, respectively. Thus, the EO logic gates of the subtractor can be shared with the equality comparator in the photonic network.

The photonic part of EPCMP is shown in Figure 1c, which is called an optical comparator network (OCMPN) in this study. An n-bit OCMPN comprises n directional couplers/splitters and $2n$ EO modulators. As shown in Figure 1d, two EO modulators along with a 2-by-2 coupler or combiner compose one bit in the OCMPN. In each bit, the optical carry signal of the previous bit c_{k-1} is first modulated by a modulator controlled by the propagating signal p_k, whereas another light beam is modulated by the generated signal g_k. These two light beams have the same wavelength and merge into the directional coupler to generate the C signal of the current bit c_k. Because light can propagate the upper arm of the directional coupler/combiner only when c_{k-1} and p_k are both logic 1s, the modulator controlled by p_k functions as an AND gate. Furthermore, the logical meanings of p_k and g_k indicate that only one input port of the combiner/directional coupler will have incoming signals because p_k and g_k cannot be

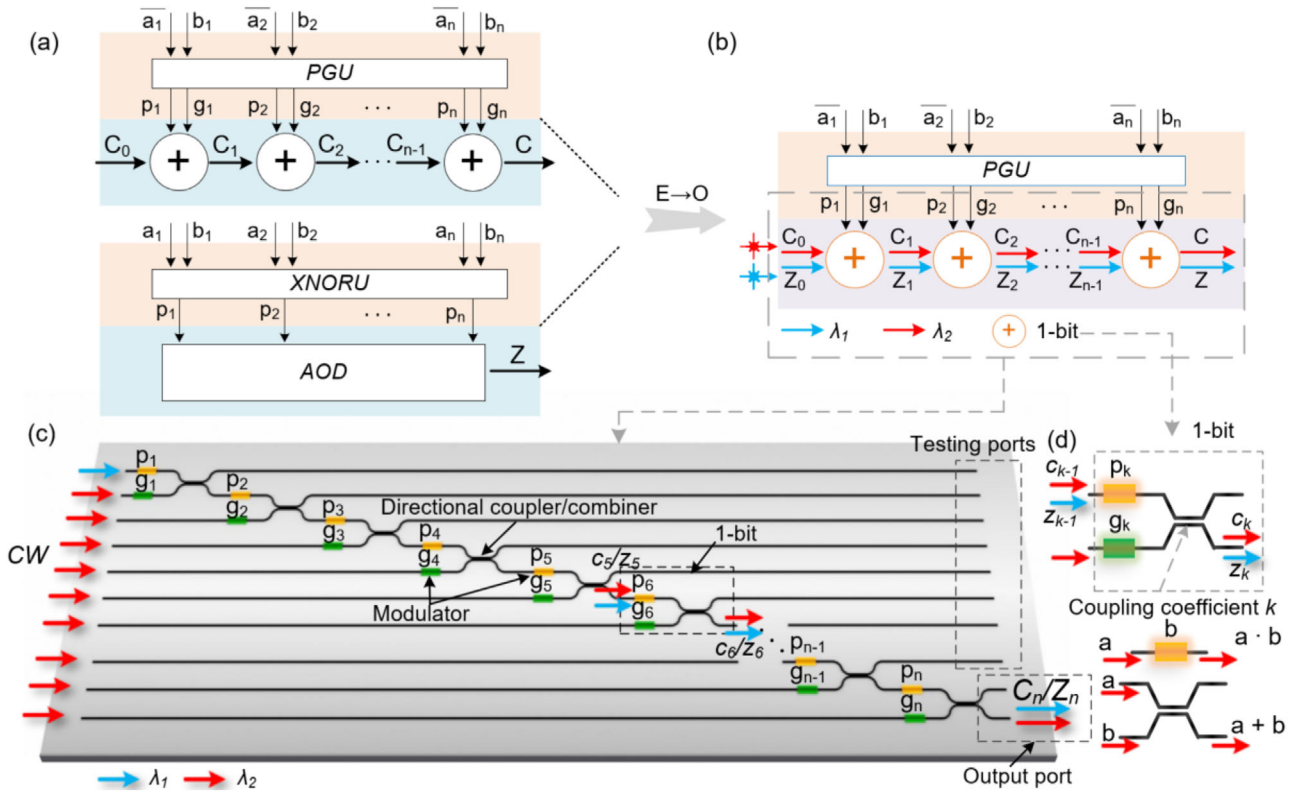

Figure 1. Schematic diagram of an electronic–photonic comparator. a) Schematic diagram of a conventional electronic comparator based on the ripple-carry full adder structure. b) General schematic diagram of the electronic–photonic comparator. The electronic critical path in (a) is replaced by optical paths, and light beams with different wavelengths will transport signals from one bit to another. c) Schematic diagram of the photonic part of WDM-based EPCMP. It consists of EO modulators and couplers/splitters. The green modulators are used for subtraction only, whereas yellow modulators are shared by the subtractor and the equality comparator. Light beams with different wavelengths generate different logic results at the output ports. The testing ports can be used for troubleshooting and wavelength alignment of the modulators. d) A diagram of one bit in the EPCMP. The logic function of each optical component is also shown. Notably, *a* and *b* cannot be both logic 1s in the directional coupler. Thus, there will be no power variations of the logic 1 signal at the output of the optical OR gate if the intensities of the optical input signals *a* and *b* are balanced.

logic 1s at the same time. Therefore, only one light beam propagates the combiner/directional coupler when $c_k = 1$, and the combiner/directional coupler functions as an OR gate. Thus, the two modulators and combiner/coupler implement Equation (1). In contrast, the light beam conveying the Z signal will only be modulated by the propagating signal p_k, and the optical components in each bit function as an AND gate.

In the EPCMP, coherent, continuous wave (CW) light beams of different wavelengths λ_1 and λ_2 are injected into different input ports of the photonic circuit: light beam λ_1 will pass through the first input port only to implement the logic of the equality comparator Z (Equation (2)), whereas light beam λ_2 will propagate the rest of the input ports to implement the logic of subtractor C (Equation (1)). The electrical signals are simultaneously injected into the modulators within each clock cycle. The intensity of lights at each input is determined by the coupling efficiency/splitting ratio of the couplers/splitters, which can be adjusted to optimize the performance of the comparator and will be discussed hereinafter. Light beams generating C and Z are separated by a demultiplexer at the output and are converted to electrical signals via photodetectors for further processing. Compared with previous designs of N-bit comparators, fewer ports are needed in an OCMPN, which can reduce the number of photodetectors and electronic components while not increasing the number of EO logic gates.[26]

3. Experimental Section

In this study, the practicality of EPCMP was experimentally demonstrated on a silicon photonics platform with a 2-bit EPCMP. The layout of the chip was drawn and verified using Phoenix OptoDesigner, and the chip was fabricated using AIM photonics with over 20 fabrication masks.

The 2-bit EPCMP comprises various passive or active components available from the AIM process design kit (PDK). Four high-speed microdisk modulators function as EO logic gates owing to their compact size and ultralow power consumption.[17] 2 × 2 50/50 directional couplers and Y branches were used to split input light to different paths or combine light from different input ports. Thermo-optic phase shifters and variable optical attenuators were deployed along the paths of each port to maintain intensity and phase balance, which are not necessary for a fine-tuned system in the future. High-speed photodetectors were placed at the output of the structure for the next-stage computation. Electrical pads placed on top of the chip were designed for thermal tuning and alignment of the microdisks, which were

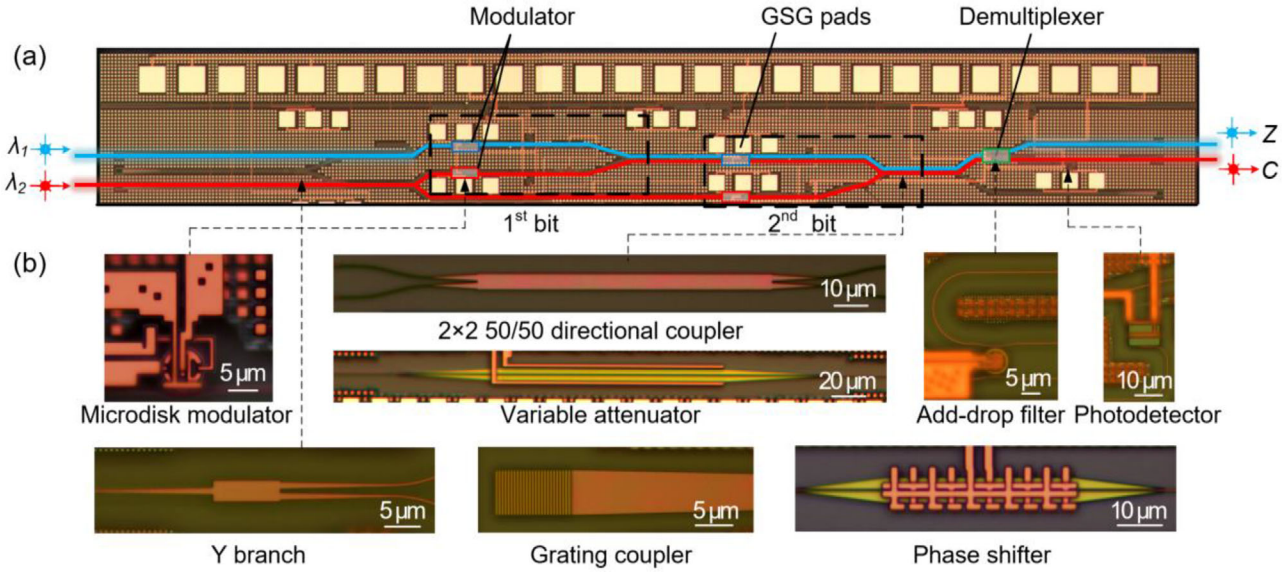

Figure 2. Optical micrographs. a) Optical micrograph of the fabricated 2-bit EPCMP, where the blue line is the path of 2-bit equality comparator, whereas the red line is the path of the 2-bit subtractor. Propagate signals (p_1, p_2) are operated on blue modulators, and generate signals (g_1, g_2) are operated on red modulators. b) Close-ups of some fundamental optical components such as Y branch, grating coupler, photodetector, phase shifter, add-drop filter (demultiplexer), 2 × 2 directional coupler, attenuator, and microdisk modulator.

wire-bonded to a printed circuit board. **Figure 2**a shows a micrograph of the fabricated EPCMP, whereas close-ups of the components are shown in Figure 2b.

The general testing procedure was as follows. First, the chip was illuminated by CW light generated by a tunable laser, which was coupled with the chip through grating couplers. Light beams with different wavelengths were launched on different grating couplers to implement different logic functions, as shown in Figure 1b. First, the resonant wavelengths of the modulators were aligned via thermal tuning. Then, the phase shifters and attenuators were adjusted to balance the phase and intensity of each arm. High-speed pseudorandom nonreturn-to-zero signals were injected into EO modulators using GSG probes. Furthermore, light beams conveying different results were separated by a fine-tuned add-drop microdisk filter. Finally, the light was coupled by grating couplers and connected to high-speed logic analyzers for testing.

The output waveforms of C and Z at two different wavelengths (≈1542 and 1567 nm) are shown in **Figure 3**. The operating wavelengths of the optical signals were chosen according to the transmission spectra of the microdisk modulators. Both functions of the subtractor and equality comparator were tested, and the relationship between the two binary inputs $A(a_2a_1)$ and $B(b_2b_1)$ could be obtained. Results obtained at operating speeds of 10 Gb s^{-1} (Figure 3a) and 20 Gb s^{-1} (Figure 3b) are shown, which are consistent with the truth table of the 2-bit comparator using the threshold detectors to read the logic of the output waveforms (see Table S2 in the Supporting Information). Additional testing details are provided in Note S1 in the Supporting Information.

Notably, the architecture was compatible with all modulators, including, but not limited to, electro-absorption modulators, MZI modulators, plasmonic modulators, and photonic crystal modulators. The performance of the architecture can also be enhanced with faster and smaller modulators, which will be discussed in the following sections.

4. Discussion

4.1. Parallel Optical Comparator Architecture

Currently, large-bit-width computations are common in commercial CPUs. For instance, 64-bit arithmetic units were put into applications decades ago.[37] To replace their electrical counterparts, we must design optical arithmetic units that can operate on large bit widths, such as 64 or 128. In our cases, the proposed optical comparator can perform large-bit-width comparisons by simply increasing the size of the photonic network. However, problems such as large propagation loss may occur because too many optical logic gates are cascaded, which will be discussed hereinafter. The latency of the EPCMP also accumulates as the bit number increases. To reduce propagation loss as well as latency, we must modify the design of the EPCMP.

Here, we suggest that an N-bit ($N = m \times n$) comparator can be decomposed into m sets of n-bit OCMPN and photodetector arrays along with electrical circuits to further reduce the total latency as well as the propagation loss in the photonic network by parallel computing, which is a widely used design strategy in VLSI. A sketch of an N-bit comparator illustrating the realization of parallel computing is presented in **Figure 4**. First, N-bit binary numbers A and B are divided into m parts, which are operated on each n-bit OCMPN simultaneously. Each OCMPN generates its outputs c_i and z_i and is received by high-speed photodetector arrays. The final carry signal C and equality comparator output Z can then be obtained by electronic modules after c_i andz_i are calculated, as depicted in Figure 4a. Because all z_i signals should be logic 1 when $A = B$ from the previous

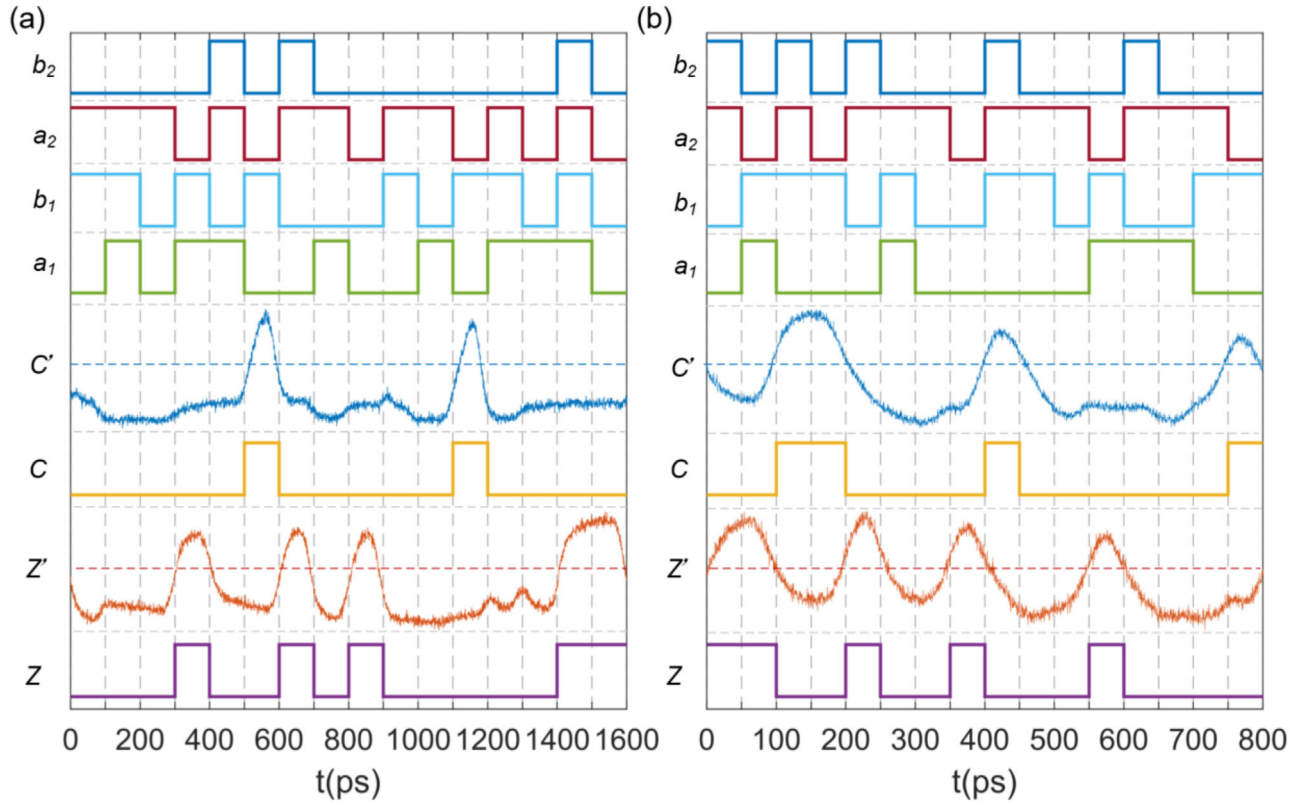

Figure 3. Testing results. The operating speeds are a) 10 Gb s^{-1} and b) 20 Gb s^{-1}. Both the original waveforms and the logic results of carry signal C (≈1542 nm) and equality signal Z (≈1567 nm) are shown. The threshold lines to detect the logic of the original waveforms are marked using blue/red dashed lines.

discussions, z_i will be the inputs of an AOD to obtain the final output of the equality comparator Z. In contrast, the output of the subtractor C will be obtained via a multiplexer with all c_i and z_i signals as inputs. For simplicity, we define $C_{i:1}/Z_{i:1}$ as the comparison results if we only compare the first $i*n$ bits of A and B. If $C_{i:1} = 1$, $(a_{i*n}a_{i*n-1}...a_2a_1) < (b_{i*n}b_{i*n-1}...b_2b_1)$, whereas if $Z_{i:1} = 1$, $(a_{i*n}a_{i*n-1}...a_2a_1) = (b_{i*n}b_{i*n-1}...b_2b_1)$. When $i = m$, $C_{m:1}/Z_{m:1}$ is the final C/Z signal in the proposed architecture. The relationship between these values can be summarized as follows

$$C_{i:1} = C_{i-1:1} \cdot z_i + c_i \tag{3}$$

$$Z = z_1 z_2 \ldots z_m \tag{4}$$

$$C = C_{m:1} \tag{5}$$

where $C_0 = 0$. (More details regarding the symbols used in this section are provided in Note S4 in the Supporting Information, and detailed design strategies and circuit diagrams are shown in Note S6 in the Supporting Information.)

In our proposed architecture, a comparison of signed inputs or floating-point inputs is also supported. The generated signals of the most significant bit (MSB) can be modified $g_{64} = a_{64} \cdot \overline{b_{64}}$ to enable signed/floating-point comparison. Note that carry signal C has different logical representations according to the signs of the input numbers, but this issue can be solved with some simple control circuits. Furthermore, with additional electrical control circuits, our EPCMP is compatible with binary inputs with different number representations (see Note S5 in the Supporting Information).

Surprisingly, an additional OCMPN can realize the functions of the AOD and the multiplexer when z_i and c_i are the electrical input signals because Equations (3) and (4) have exactly the same form as Equations (1) and (2). The hybrid electronic–photonic MUX/AOD module is shown in Figure 4b, whereas the OCMPN is shown in Figure 4c.

Here, we believe that the OCMPN-based electronic–photonic MUX/AOD outperforms the conventional electrical MUX/AOD in terms of latency and power consumption. First, we reduce the number of logic gates to realize the functions of MUX and AOD using a two-wavelength-based WDM, which also leads to lower power consumption. Second, the speed of the EPCMP is further improved because C and Z can be calculated in sub-picoseconds after c_i and z_i signals are applied on the OCMPN. The only problem is that an additional OE–EO conversion is required, which may reduce the entire latency of the N-bit comparator. However, the conversion speed and efficiency of the OE–EO conversion have been dramatically improved in recent studies.[38] Furthermore, OE–EO conversion can be avoided if the EO logic gates in the OCMPN are replaced by all optic logic gates.

Finally, C and Z were processed to obtain the relationship between A and B. The entire architecture, including electronic and photonic modules, can be fabricated on a single chip using modern fabrication technology.[7]

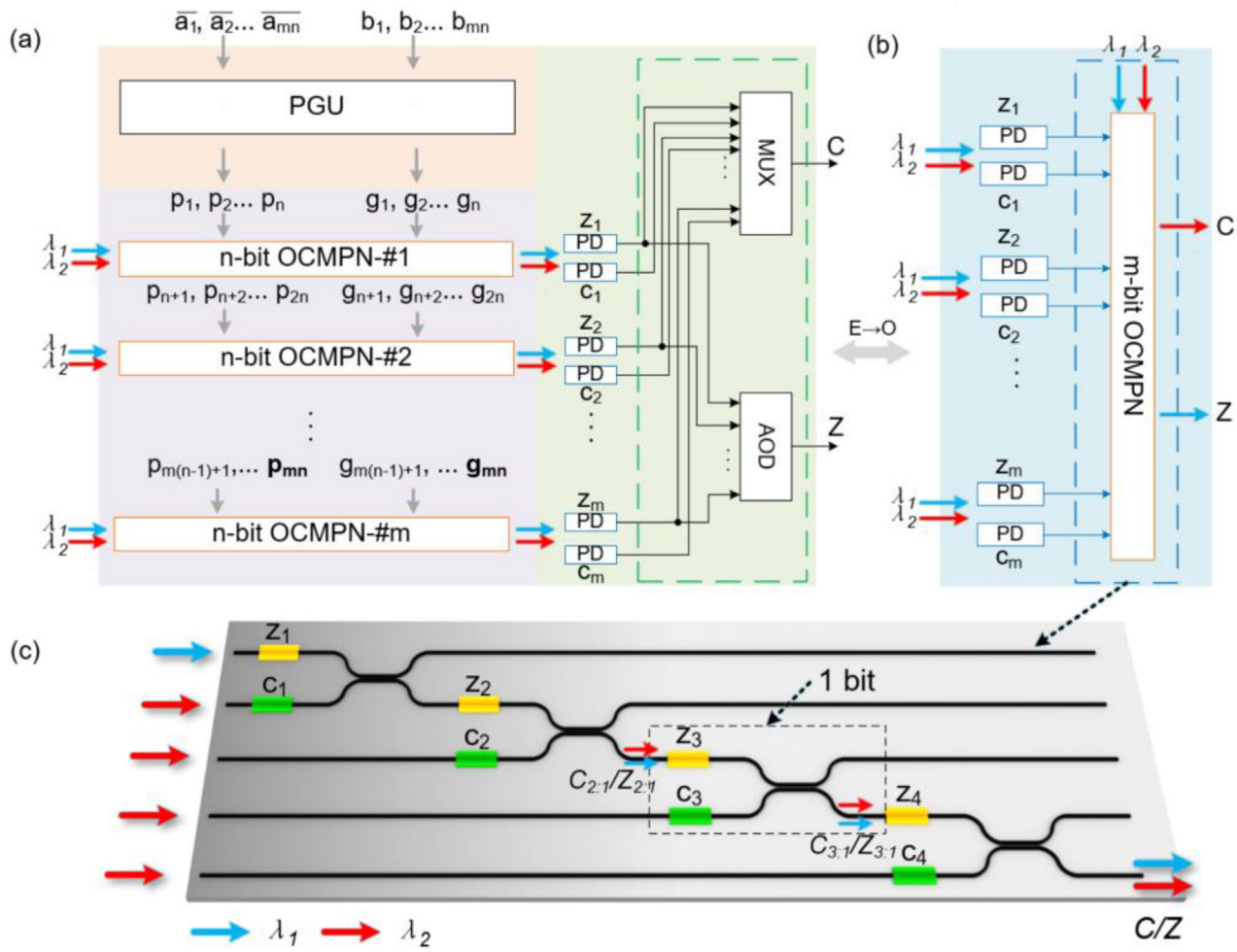

Figure 4. Schematic diagram of the parallel EPCMP architecture. It consists of a (*p*,*g*) generation unit (PGU), *m* sets of *n*-bit OCMPNs, an array of high-speed photodetectors (PDs) along with an electronic multiplexer, and an AOD shown in (a) or an OCMPN shown in (b). The *p* and *g* signals at MSB (the m^*n^{th} bit) is bolded, and they will be altered to handle different input formats. c) Schematic diagram of an *m*-bit OCMPN ($m = 4$) to implement functions of multiplexers and AODs using WDM. $C_{i:1}/Z_{i:1}$ are group *C*/*Z* signals (*i* is an integer, $i \leq m$).

4.2. Computational Speed

The proposed EPCMP utilizes light to process information in the critical path in sub-picoseconds, which is one or two orders of magnitude faster than electrical gates. The propagation delay of electrical gates is determined by the charging/discharging time of transistors and metal wires for interconnects.[30] Moreover, the fan-out and loads reduce the speed of the electrical gates. In contrast, the delay of optical gates in our EPCMP is caused by the propagation time of light in the optical path, and it will not be affected by the fan-out or loads. Thus, the computing speed of EPCMP is much higher than that of electronic comparators. The time latency of an *N*-bit ($N = m \times n$) parallel prefix comparator includes the EO time constant of the modulator τ_{eo}, the latency of the electrical signal τ_g, the latency of each optical OR gate τ_o, the optoelectronic transition time for PDs τ_{oe}, and the electrical delay in the AOD as well as the MUX within one stage τ_e . The total latency can then be expressed as follows

$$\tau = \tau_c + n \times \tau_o + \log_2 m \times \tau_e \quad (6)$$

where $\tau_c = \tau_{eo} + \tau_g + \tau_{oe}$ is a constant, and $\log_2 m$ is the number of stages required for an MUX and all-ones detector, which can be realized by tree structures. We assume that $\tau_g$and $\tau_e$for electronic gates are both 7 ps in state-of-the-art 7 nm technology,[39] τ_{eo} and τ_{oe} for EO/OE conversion are 10 ps,[40,41] and τ_o is 0.3 ps.[42] The results presented in **Figure 5** indicate that a 64-bit EO comparator can operate at over 20 Gb s^{-1} and can proceed faster because of improvements in the active and passive components in the architecture. As a comparison, the operating speed of an electronic comparator can reach ≈4 Gb s^{-1} because the operating speed is limited by the maximum clock rate of transistors.[32,43]

The latency and efficiency of OE–EO conversion dominate the total latency of the architecture, as shown in Figure 4b, where the electronic multiplexers and all-ones detectors are replaced by an OCMPN. The total latency can be written as follows

$$\tau = \tau_c + (n + m) \times \tau_o + \tau_{eo} + \tau_{oe} \quad (7)$$

where an additional OE/EO conversion is required. Figure 4b will outperform the architecture shown in Figure 4a once the latency

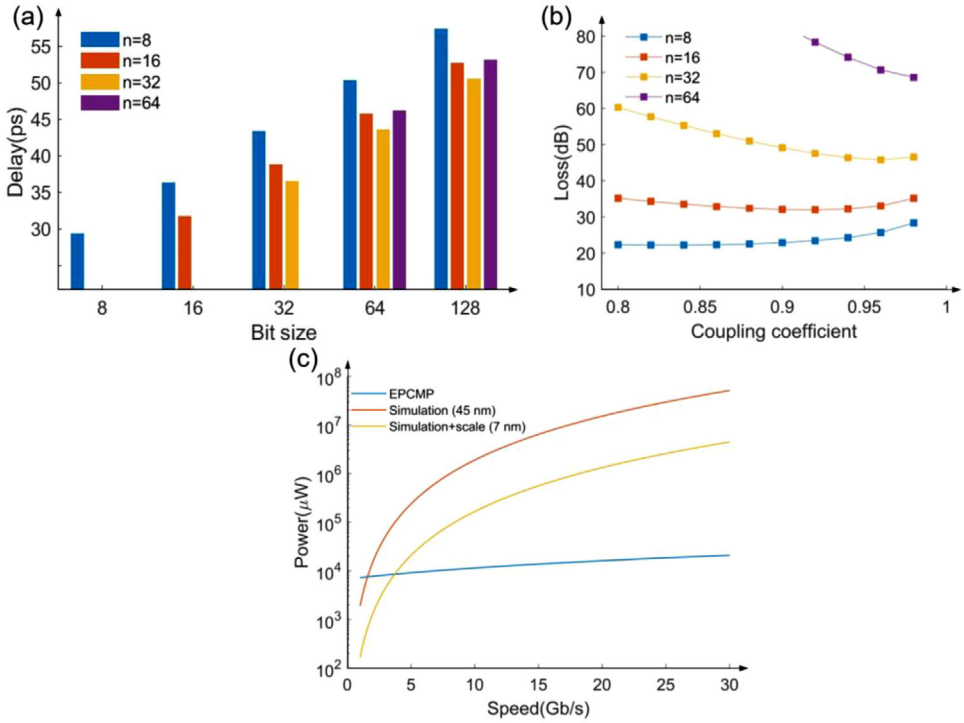

Figure 5. Performance analysis. a) The entire delay of the EPCMP with respect to the bit size *N*; the delay of EPCMP with different *n*-bit OCMPNs is also shown. b) The propagation loss of a 64-bit EPCMP with respect to the coupling coefficient of each directional coupler; the optimized coupling coefficient for different bit size *n* is shown. c) The power consumption of a 64-bit EPCMP ($m = 8$, $n = 8$, coupling coefficient = 0.8) in terms of the operating speed and the performance of the electrical counterparts are also shown for comparison.

τ_{eo}/τ_{oe}can be further reduced by comparing Equations (6) and (7)[38,44] (see Note S7 in the Supporting Information).

4.3. Loss

Light experiences loss while propagating through the optical route because of splitters, insertion loss of EO modulators, and waveguides, which accumulate in the optical critical path as the bit number increases. Although on-chip amplifiers are available on some platforms (InP) and can be grown on a silicon photonics platform,[45] they consume considerable power to boost the signal.

The loss of an EPCMP can be optimized by changing the coupling efficiency/splitting ratio of the directional coupler/combiner, as shown in Figure 5b. Because there is only one output port, one must optimize the loss among all possible optical paths that will propagate the output port, among which the critical path is the lossiest part for it to propagate all couplers and EO modulators. Our calculation shows that the optical loss can be optimized to below 30 dB in a 64-bit comparator, which indicates that our comparator can implement large-bit-size comparisons without amplifiers (see Note S8 in the Supporting Information).

4.4. Energy Efficiency

Energy has constrained the design of electronic computing devices because the power consumption of a transistor-based circuit has a positive correlation with f^3 (f is the clock frequency).[37] In comparison, optical circuits only consume energy proportional to f,[17] and various energy-efficient components have been investigated; for example, the microdisk modulator in experimental demonstration achieves approximately 1 fJ per bit. A detailed evaluation of the energy efficiency of OCMPNs has been performed in previous studies, which have revealed that the power consumption of optical adders can be one to two orders of magnitude smaller than that of their electrical counterparts.[24] The conclusion is also general to comparators, which are OCMPN-based structures. Moreover, a two-wavelength-based WDM is utilized to optimize the complexity of photonic circuits, which allows us to minimize the number of active components in the EPCMP. The following equation can be used to estimate the power consumption of the EPCMP

$$P_{\text{total}} = \alpha(P_{\text{PGU}} + N_{\text{md}}P_{\text{md}}) + N_{\text{OCMPN}}\frac{P_{\text{min}}}{\eta \text{IL}_{\text{OCMPN}}} \tag{8}$$

where α is the activating coefficient of the EPCMP, P_{PGU} is the power to propagate and generate signals, N_{md} is the total number of EO modulators in the EPCMP, P_{md} is the power consumption of each modulator, N_{OCMPN} is the number of OCMPNs for constructing the *N*-bit EPCMP, P_{min} is the minimum detectable power of the photodetector, η is the wall-plug efficiency of the laser, and IL_{OCMPN} is the propagation loss of the entire OCMPN. For each bit, the power consumption of the modulators and the logic gates to drive the modulators is approximately $6C_{\text{md}}V^2f$ (the

details to obtain this value are provided in Note S9 and Table S6 in the Supporting Information), where C_{md} is the capacitance of the modulator, and V is the operating voltage. Figure 5c shows a comparison between our EPCMP and a purely electrical 64-bit comparator based on 45 and 7 nm technology nodes in terms of power consumption. We first used a commercial Synopsys Design Compiler (version 2017) to simulate the performance of the electrical comparator based on a 45 nm technology node (gscl45nm). Then, the performance of the decoder in the 7 nm technology node was calculated using scaling equations. More details regarding the evaluation of the power consumption of the EPCMP are provided in Note S9 in the Supporting Information.

Figure 5c reveals that when operating at tens of Gb s^{-1}, the power consumption of the EPCMP can be approximately two orders of magnitude better than its electrical counterpart. For instance, the EPCMP consumes 82 times less power than its electrical counterparts when it is operated at 20 Gb s^{-1}. The advantages of using the EPCMP for processing information will be expanded when it operates on a larger bit number because electrical circuits will suffer from more severe interconnection issues when the number of transistors increases.

5. Outlook

As discussed, the proposed N-bit EPCMP outperforms its electrical counterparts in terms of speed and energy efficiency. The performance metrics of the EPCMP can be further improved in several directions. The improvement strategies are also valid for other direct-logic-based computing modules.

First, the performance and footprint of EPCMP can be enhanced by using better passive and active components in the architecture. For example, shorter splitters and smaller EO modulators with dimensions of a few square micrometers will reduce the length of the optical path as well as the total optical propagation latency.[16,46,47] Modulators consuming sub-femtojoules per bit have also been experimentally demonstrated recently. [16]

Second, we believe that a faster conversion speed between electrical and optical signals will lead to a lower latency of the EPCMP. Equation (7) and Figure 5 show that $\tau_{eo}$and τ_{eo} contribute a constant time delay, which limits the computing speed of an EPCMP, especially for low-bit computation. With faster EO/OE conversion techniques, more electrical components can be replaced by optical circuits, and more complicated optical computing modules can be designed.

Finally, more design techniques specified for optical circuits can be explored, which will optimize the performance of the optical computing module at the architectural level. For instance, more wavelengths for multiplexing techniques can be introduced in optical circuit design, which can further reduce the number of required EO logic gates. There are also some novel building blocks, such as multioperand logic gates, where multiple inputs can be injected into a single EO modulator to realize various logic functions.[48] We believe that the size and the latency can be further reduced if they are used as basic building blocks.

6. Conclusion

We present a novel electronic–photonic digital comparator with an experimental demonstration at 20 Gb s^{-1}. A two-wavelength-based WDM (1542 and 1567 nm in experiments) was used to reduce the number of modulators, scale down the size, and reduce the power consumption of the architecture. Using EO and optical logic gates, high-speed computation was achieved with lower power consumption in a compact architecture. The performance of our architecture can be further improved by developing modulators, photodetectors, and OE–EO conversion techniques. More advanced architectures are expected to be designed if more advanced optical interconnects, EO, or all-optical logic gates are investigated.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

digital comparator, electronic–photonic, high-speed, wavelength-division-multiplexing

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[1] M. M. Waldrop, *Nature* **2016**, *530*, 144.
[2] R. H. Dennard, F. H. Gaensslen, Y. U. Hwa-Nien, V. L. Rideout, E. Bassous, A. R. Leblanc, *Proc. IEEE* **1999**, *87*, 668.
[3] J. Zou, F. Zhao, R. T. Chen, *J. Light Technol.* **2005**, *23*, 2926.
[4] J. Qiao, F. Zhao, R. T. Chen, J. W. Horwitz, W. W. Morey, *Appl. Opt.* **2002**, *41*, 6567.
[5] R. T. Chen, L. Lin, C. Choi, Y. J. Liu, B. Bihari, L. Wu, S. Tang, R. Wickman, B. Picor, M. K. Hibbs-Brenner, J. Bristow, Y. S. Liu, *Proc. IEEE* **2000**, *88*, 780.
[6] Y. Zhang, A. Hosseini, X. Xu, D. Kwong, R. T. Chen, *Opt. Lett.* **2013**, *38*, 3608.
[7] C. Sun, M. T. Wade, Y. Lee, J. S. Orcutt, L. Alloatti, M. S. Georgas, A. S. Waterman, J. M. Shainline, R. R. Avizienis, S. Lin, B. R. Moss, R. Kumar, F. Pavanello, A. H. Atabaki, H. M. Cook, A. J. Ou, J. C. Leu, Y.-H. Chen, K. Asanović, R. J. Ram, M. A. Popović, V. M. Stojanović, *Nature* **2015**, *528*, 534.

[8] A. H. Atabaki, S. Moazeni, F. Pavanello, H. Gevorgyan, J. Notaros, L. Alloatti, M. T. Wade, C. Sun, S. A. Kruger, H. Meng, K. Al Qubaisi, I. Wang, B. Zhang, A. Khilo, C. V. Baiocco, M. A. Popović, V. M. Stojanović, R. J. Ram, *Nature* **2018**, *556*, 349.
[9] J. Hardy, J. Shamir, *Opt. Express* **2007**, *15*, 150.
[10] C. Qiu, X. Ye, R. Soref, L. Yang, Q. Xu, *Opt. Lett.* **2012**, *37*, 3942.
[11] D. R. Solli, B. Jalali, *Nat. Photonics* **2015**, *9*, 704.
[12] Y. Tian, L. Zhang, R. Ji, L. Yang, Q. Xu, *Opt. Lett.* **2011**, *36*, 3795.
[13] Y. Shen, N. C. Harris, S. Skirlo, M. Prabhu, T. Baehr-Jones, M. Hochberg, X. Sun, S. Zhao, H. Larochelle, D. Englund, M. Soljacic, *Nat. Photonics* **2017**, *11*, 441.
[14] S. A. Srinivasan, M. Pantouvaki, S. Gupta, H. T. Chen, P. Verheyen, G. Lepage, G. Roelkens, K. Saraswat, D. Van Thourhout, P. Absil, J. Van Campenhout, *J. Light Technol.* **2016**, *34*, 419.
[15] C. Wang, M. Zhang, X. Chen, M. Bertrand, A. Shams-Ansari, S. Chandrasekhar, P. Winzer, M. Lončar, *Nature* **2018**, *562*, 101.
[16] W. Heni, Y. Fedoryshyn, B. Baeuerle, A. Josten, C. B. Hoessbacher, A. Messner, C. Haffner, T. Watanabe, Y. Salamin, U. Koch, D. L. Elder, L. R. Dalton, J. Leuthold, *Nat. Commun.* **2019**, *10*, 1694.
[17] E. Timurdogan, C. M. Sorace-Agaskar, J. Sun, E. Shah Hosseini, A. Biberman, M. R. Watts, *Nat. Commun.* **2014**, *5*, 4008.
[18] C. Peng, J. Li, H. Liao, Z. Li, C. Sun, J. Chen, Q. Gong, *ACS Photonics* **2018**, *5*, 1137.
[19] L. Zhang, R. Ji, L. Jia, L. Yang, P. Zhou, Y. Tian, P. Chen, Y. Lu, Z. Jiang, Y. Liu, Q. Fang, M. Yu, *Opt. Lett.* **2010**, *35*, 1620.
[20] Q. Xu, R. Soref, *Opt. Express* **2011**, *19*, 5244.
[21] C. Feng, Z. Ying, Z. Zhao, R. Mital, D. Z. Pan, R. T. Chen, *IEEE J. Sel. Top. Quantum Electron.* **2019**, *26*, 1.
[22] Z. Ying, Z. Wang, Z. Zhao, S. Dhar, D. Z. Pan, R. Soref, R. T. Chen, *Opt. Lett.* **2018**, *43*, 983.
[23] A. Shinya, T. Ishihara, K. Inoue, K. Nozaki, S. Kita, M. Notomi, *Optical Data Science: Trends Shaping the Future of Photonics. International Society for Optics and Photonics* **2018**, *10551*, 1055106.
[24] Z. Ying, C. Feng, Z. Zhao, S. Dhar, H. Dalir, J. Gu, Y. Cheng, R. Soref, D. Z. Pan, R. T. Chen, *Nat. Commun.* **2020**, *11*, 2154.
[25] L. Yang, C. Guo, W. Zhu, L. Zhang, C. Sun, *IEEE Photonics Technol. Lett.* **2015**, *27*, 809.
[26] D. Gostimirovic, W. N. Ye, *Sci. Rep.* **2017**, *7*, 12603.
[27] Z. Zhao, D. Liu, Z. Ying, B. Xu, C. Feng, R. T. Chen, D. Z. Pan, in *2019 Design, Automation & Test in Europe Conference & Exhibition (DATE), IEEE*, **2019**, pp. 1567–1570.
[28] Z. Ying, Z. Zhao, C. Feng, R. Mital, S. Dhar, D. Z. Pan, R. Soref, R. T. Chen, *Opt. Express* **2018**, *26*, 28002.
[29] Z. Ying, Z. Wang, Z. Zhao, S. Dhar, D. Z. Pan, R. Soref, R. T. Chen, *Opt. Lett.* **2018**, *43*, 983.
[30] N. Weste, D. M. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, 4th ed., Pearson, New York **2010**.
[31] S. Abdel-Hafeez, A. Gordon-Ross, B. Parhami, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2013**, *21*, 1989.
[32] C. Efstathiou, K. Dimolikas, C. Papaioannou, Y. Tsiatouhas, in 2018 25th IEEE Int. Conf. *on Electronics Circuits and Systems (ICECS), IEEE*, **2019**, p. 249.
[33] B. Nakarmi, M. Rakib-Uddin, Y. H. Won, *J. Light Technol.* **2011**, *29*, 3015.
[34] P. Sethi, S. Roy, *IEEE J. Sel. Top. Quantum Electron.* **2013**, *20*, 118.
[35] Y. Tian, H. Xiao, X. Wu, Z. Liu, Y. Meng, L. Deng, X. Guo, G. Liu, J. Yang, *Nanophotonics* **2018**, *7*, 669.
[36] R. Patil, V. Agarwal, in 2017 *Int. Conf. on Computing, Communication, Control and Automation (ICCUBEA 2017), IEEE*, **2017**, pp. 1–5.
[37] S. K. Mathew, M. A. Anders, B. Bloechel, T. Nguyen, R. K. Krishnamurthy, S. Borkar, *IEEE J. Solid-State Circuits* **2005**, *40*, 44.
[38] K. Nozaki, S. Matsuo, T. Fujii, K. Takeda, A. Shinya, E. Kuramochi, M. Notomi, *Nat. Photonics* **2019**, *13*, 454.
[39] A. Stillmaker, B. Baas, *Integration* **2017**, *58*, 74.
[40] G. T. Reed, G. Z. Mashanovich, F. Y. Gardes, M. Nedeljkovic, Y. Hu, D. J. Thomson, K. Li, P. R. Wilson, S. W. Chen, S. S. Hsu, *Nanophotonics* **2014**, *3*, 229.
[41] L. Vivien, A. Polzer, D. Marris-Morini, J. Osmond, J. M. Hartmann, P. Crozat, E. Cassan, C. Kopp, H. Zimmermann, J. M. Fédéli, *Opt. Express* **2012**, *20*, 1096.
[42] Z. Ying, S. Dhar, Z. Zhao, C. Feng, R. Mital, C.-J. Chung, D. Z. Pan, R. A. Soref, R. T. Chen, *IEEE J. Sel. Top. Quantum Electron.* **2018**, *24*, 1.
[43] M. Ghasemzadeh, S. Najafibisfar, A. Amini, in *2018 25th International Conference Mixed Design of Integrated Circuits and System (MIXDES), IEEE*, **2018**, p. 215–217.
[44] J. K. George, A. Mehrabian, R. Amin, J. Meng, T. F. de Lima, A. N. Tait, B. J. Shastri, T. El-Ghazawi, P. R. Prucnal, V. J. Sorger, *Opt. Express* **2019**, *27*, 5181.
[45] S. Liu, J. Norman, M. Dumont, D. Jung, A. Torres, A. C. Gossard, J. E. Bowers, S. Liu, A. Torres, A. Gossard, J. Bowers, S. Liu, D. Jung, A. Gossard, J. Bowers, J. Norman, M. Dumont, A. Gossard, J. Bowers, D. Jung, *ACS Photonics* **2019**, *6*, 2523.
[46] C. Haffner, D. Chelladurai, Y. Fedoryshyn, A. Josten, B. Baeuerle, W. Heni, T. Watanabe, T. Cui, B. Cheng, S. Saha, D. L. Elder, L. R. Dalton, A. Boltasseva, V. M. Shalaev, N. Kinsey, J. Leuthold, *Nature* **2018**, *556*, 483.
[47] Y. Liu, Z. Li, S. Wang, N. Zhang, Y. Yao, J. Du, Z. He, Q. Song, K. Xu, in *2019 Optical Fiber Communications Conf. and Exhibition (OFC), IEEE*, **2019**, pp. 1–3.
[48] Z. Ying, C. Feng, Z. Zhao, R. Soref, D. Pan, R. T. Chen, *Appl. Phys. Lett.* **2019**, *115*, 171104.