Research article

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# Wavelength-division-multiplexing (WDM)-based integrated electronic–photonic switching network (EPSN) for high-speed data processing and transportation

High-speed optical switching network

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**Abstract:** Integrated photonics offers attractive solutions for realizing combinational logic for high-performance computing. The integrated photonic chips can be further optimized using multiplexing techniques such as wavelength-division multiplexing (WDM). In this paper, we propose a WDM-based electronic–photonic switching network (EPSN) to realize the functions of the binary decoder and the multiplexer, which are fundamental elements in microprocessors for data transportation and processing. We experimentally demonstrate its practicality by implementing a 3–8 (three inputs, eight outputs) switching network operating at 20 Gb/s. Detailed performance analysis and performance enhancement techniques are also given in this paper.

**Keywords:** decoder; electronic–photonic; high-speed; multiplexer; WDM.

## 1 Introduction

Using light to carry out computation tasks on a chip is intriguing these years thanks to the critical features of light, which are low latency and high bandwidth [1–5]. Computation with integrated photonic circuits has the potential to replace transistor-based electrical circuits, which suffer from overwhelming heat and physical limits as speed and power consumption per bit are close to saturation [6, 7]. Moreover, current fabrication technologies allow photonic components and transistors to be integrated on the same chip, which paves the way for interchip and intrachip communications [8, 9] between electronic and photonic modules to realize some complex computing modules [10, 11].

With advanced fabrication technologies as mentioned above, researchers pay significant attention to replacing electrical combinational logic circuits based on very large-scale integration (VLSI) technology with photonic counterparts. Researchers investigated abundant passive and active building blocks for optical computing and interconnect on integrated photonic platforms such as electro-optic (EO) switches and modulators [12–15]. Most of them are available from the foundries currently. Then, optical digital logic gates [16–19] and basic arithmetic units, including but not limited to adders [20, 21], comparators [22, 23], encoders [4], and decoders [24], are designed. They are all essential parts of an arithmetic logic unit (ALU) [25]. Besides, logic synthesis specified for photonic circuits has been put forward for designing more sophisticated computing modules [26, 27].

As numerous optical arithmetic units in the ALU have been proposed for speeding up the execution stage of the instruction cycle, accelerating other stages is also essential for the performance enhancement of the whole microprocessor. From the computer architecture point of view, the ALU is controlled by the instructions from the control unit, while the input data of the ALU come from the memory [28]. After the ALU implements one function, the output will then be stored in the memory for future computations. When the latency of the ALU can be dramatically reduced

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by replacing electrical computing modules with optical counterparts, the bottleneck that may slow down the speed of the entire microprocessor lies in the data transportation and processing among the ALU, controlling unit, and the memory, which will suffer from interconnection problems as the clock rate goes up if we still use metal wires for data transportation [29]. In order to enhance the speed, as well as the efficiency, of data transportation between the ALU and other modules in the microprocessor, we intend to design photonic circuits that are capable of implementing high-speed data transmission and some simple data processing tasks.

Decoders and multiplexers are crucial combinational logic circuits for data processing among modules. They are widely used for data selection, demultiplexing, decoding in various parts in a microprocessor [30]. The logic functions of transistor-based electrical decoders and multiplexers are quite straightforward, and few optimization methods can be applied to the circuit design. In the optical domain, several structures can realize the functions of the binary decoder [31]. However, there is much potential for us to optimize the design, which will be discussed hereinafter.

In this paper, we devise the architecture of a scalable wavelength-division multiplexing (WDM)–based electronic–photonic switching network (EPSN) for accelerating the inner module or intramodule data transportation and processing in different microprocessors, including but not limited to general-purpose processors, field-programmable gate arrays (FPGAs), and application-specific integrated circuits (ASICs). This proposed network can realize the functions of binary decoders and multiplexers. WDM is used to reduce the footprint, as well as the power consumption, of the device. A 3–8 decoder operating at 20 Gb/s is also experimentally demonstrated. Last but not least, a detailed performance evaluation of our EPSN and further optimization methods are discussed.

# 2 Theory and architecture

## 2.1 Decoder/multiplexer in computer architecture

Figure 1 shows the modules of a von Neumann architecture, where the applications of decoders and multiplexers are disclosed to our best knowledge. More details of the microprocessor can be found in supplementary material (see Supplementary S1). Firstly, decoders are used to decode the program instructions such as opcodes to activate the specific module in the ALU and to obtain the data coming from the memory for execution. After the ALU performs operations on the data, the computed results will be stored in specific locations of the memory part by decoders and multiplexers. Therefore, the decoders and multiplexers are widely used to transport and process data between different modules in a microprocessor. In a directed logic–based architecture, the electronic–photonic ALU (EPALU) is controlled by electrical control units, and the data it calculated will also be stored in the memory. Therefore, the roles of decoders and multiplexers will remain unchanged in electronic–photonic microprocessors (EPMs).

However, if we still use electrical decoders and multiplexers for data transporting between different modules in the EPALU or EPM, the performance of the whole microprocessor will be deteriorated. Firstly, a binary decoder, which converts a binary input code to a decimal output code, will have $n$ binary input signals and will generate $2^n$ outputs. $2^n$ input signals and $2^n$ $n$-bit AND gates are required to construct a decoder/multiplexer. As the bit number increases, the electrical decoder will suffer from fan-in issues, and the delay of each bit will accumulate. Furthermore, because the EPALU is larger than the transistor-based electrical ALU [25], the distance of the data transportation between the EPALU and other modules is also longer than that of electrical ALUs. Therefore, the interconnect problems will emerge or even be worse than those of pure electrical microprocessors if we still use metal wires to connect among different modules. The speed and energy consumption of data transportation will be the bottleneck of the EPM. Intending to improve the performance of data transportation, we design optical decoders and multiplexers for high-speed and energy-efficient data transportation and processing. It is interesting that the functions of the decoder and the multiplexer can be realized in the same photonic circuit, which is named the EPSN by us.

## 2.2 WDM-based electronic–photonic switching network

The scheme of a WDM-based EPSN is shown in Figure 1(c) and (d), which consists of splitters, EO modulators, and add-drop filters. We first illustrate the mechanism of this network when it functions as a decoder: The optical decoder is a tree-like structure, the node of which is composed of an EO modulator controlling the flow of the light beam. Starting from the root node, each node will be connected with two child nodes via a Y branch. In the end, each terminal node will be followed by an add-drop filter,

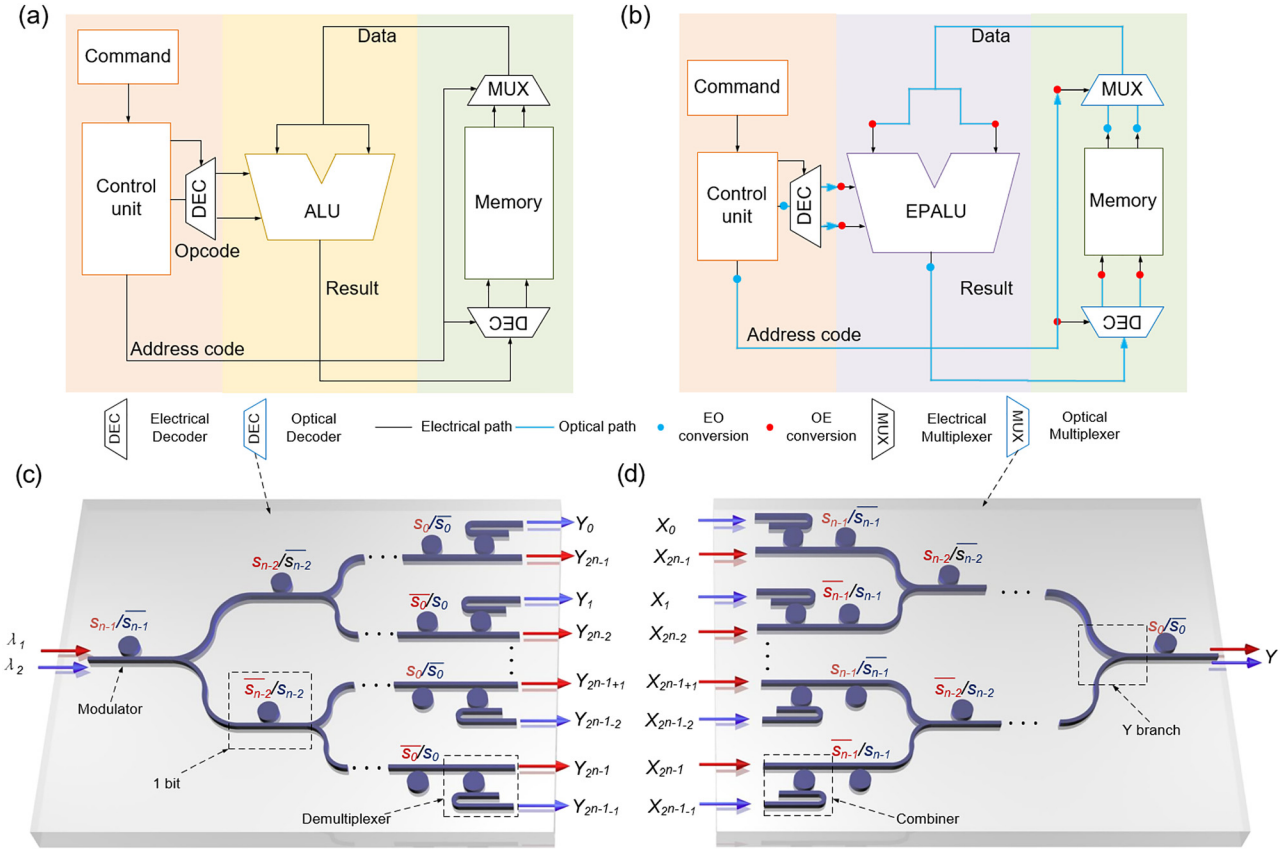


**Figure 1:** Schematic of a von Neumann architecture.
The functions of decoders and multiplexers are emphasized. It should be noted that the real circuits are more complicated. (a) Schematic of a conventional electronic microprocessor where all the modules are electrical circuits. (b) An electronic–photonic microprocessor. The electrical arithmetic logic unit (ALU) is replaced by a directed logic–based electronic–photonic ALU (EPALU), which is controlled by the electrical controlling unit. Besides, we use electronic–photonic decoders and multiplexers to transport and process data. (c) Schematic of an $n$–$2^n$ ($n$ inputs, $2^n$ outputs) electronic–photonic decoder (EPDEC). (d) Schematic of a $2^n$–$n$ ($2^n$ inputs, $n$-bit control signal, 1 output) electronic–photonic multiplexer (EPMUX). In (c) and (d), $s_i$ refers to the electrical input signal, and $Y$ or $Y_i$ is the optical output signal. $X_i$ is the optical input signal in (d).

which will finally split the input light beam to $2^n$ optical paths. According to the electrical input signals, which are operated on the EO modulators simultaneously within each clock cycle, light can only exit one output port while the rest of the light beams will be cut off by modulators. In the end, the optical signals can be converted to electrical signals with high-speed photodetectors (PDs) for the next stage instruction/computation [32].

Here, we use two light beams with different wavelengths, $\lambda_1$ and $\lambda_2$, to convey information. The operational wavelengths, $\lambda_1$ and $\lambda_2$, are carefully chosen according to the transmission spectrum of EO modulators to transmit different logic functions which are inverse codes to each other. The two light beams will be separated by add-drop filters or other optical demultiplexers at the end of each output port. The advantage of using WDM is that the number of EO logic gates can be reduced. Using one wavelength, we will need $2^{n+1}$–1 modulators to implement the $n$–$2^n$ binary decoder with our structure. After using WDM, however, only $2^n$–1 modulators are needed to implement the same logic function. Therefore, 50% of EO logic gates can be reduced using WDM. As a result, the footprint, as well as the total power consumption of the EPSN, can also be reduced by one half.

Owing to the bidirectional feature of linear optics, our proposed EPSN can also function as an electronic–photonic multiplexer (EPMUX) once the input ports and outputs are reversed. The scheme of the EO MUX is disclosed in Figure 1(d). In the EO MUX, $2^n$ light beams with wavelengths $\lambda_1$ or $\lambda_2$ will enter the structure. Controlled by the $n$-bit controlling electrical signals $S_n$, $S_{n-1}$ … $S_0$, only the light beam that is selected will propagate the output port, while the others will be cut off by EO modulators. Same as the optical decoder, using WDM will also help us save 50% of EO modulators compared to the EPMUX that only uses one wavelength to convey information.

It should be pointed out that our EPSN is compatible with any narrowband modulators including but not limited to plasmonic modulators and photonic crystal (PhC) modulators [14, 33]. The performance of the architecture will also be enhanced with faster and smaller modulators, which will be discussed in the following discussions. EO logic gates can also be replaced by all-optical logic gates to reduce the number of optical–electrical (OE)/EO conversions.

# 3 Experiment

In this paper, we experimentally demonstrate the practicality of the EPSN on the silicon photonics platform with a 3–8 binary decoder. The layout of the chip was drawn and verified using Synopsys OptoDesigner (version 2018) while the chip was fabricated by American Institute for Manufacturing (AIM) Integrated Photonics with over 20 photomasks.

Figure 2 shows the schematic of the 3–8 decoder, which is composed of various passive and active components [34]. Seven high-speed microdisk modulators function as EO logic gates owing to their compact size and ultralow power consumption [15]. Y branches (multimode interferometers) will split input light to different output ports, where demultiplexers (add-drop filters) are deployed to separate light beams of different wavelengths. Electrical pads sitting on the bottom of the chip are designed for thermal tuning and wavelength alignment of the microdisks, which are wire bonded to a printed circuit board (PCB).

The general testing procedure is shown as follows: Firstly, the chip is illuminated by continuous wave (CW) light generated by a tunable laser, which is coupled into the chip through grating couplers. Then, the resonant wavelengths of modulators are aligned via thermal tuning. High-speed pseudorandom non return-to-zero (NRZ) signals will be injected into EO modulators via ground-signal-ground (GSG) probes. Furthermore, light beams of different wavelengths will be separated by a fine-tuned add-drop microdisk filter. In the end, the light beams will be coupled out by grating couplers and be connected to high-speed logic analyzers for testing.

The testing logics of eight outputs at two different wavelengths are depicted in Figure 3(a) and (b), respectively, (~1542 and 1566.8 nm) according to the transmission spectra of microdisk modulators. Here, we use threshold lines to detect the logic of the output waveform and compare the measured results with the truth table of the decoder. There are eight output ports in total, and the results of them with the operating speed of 10 and 20 Gb/s are shown, which are consistent with the truth table of the 3–8 decoder. More details of testing can be found in supplementary material (see Supplementary S2).

# 4 Discussion

## 4.1 Scalable $N$–$2^N$ optical decoder

Large-bit size instruction in required in commercial CPUs. For instance, $2^{24}$ addresses are needed if the address codes of the microprocessor are 3 bytes (24 bits), which is

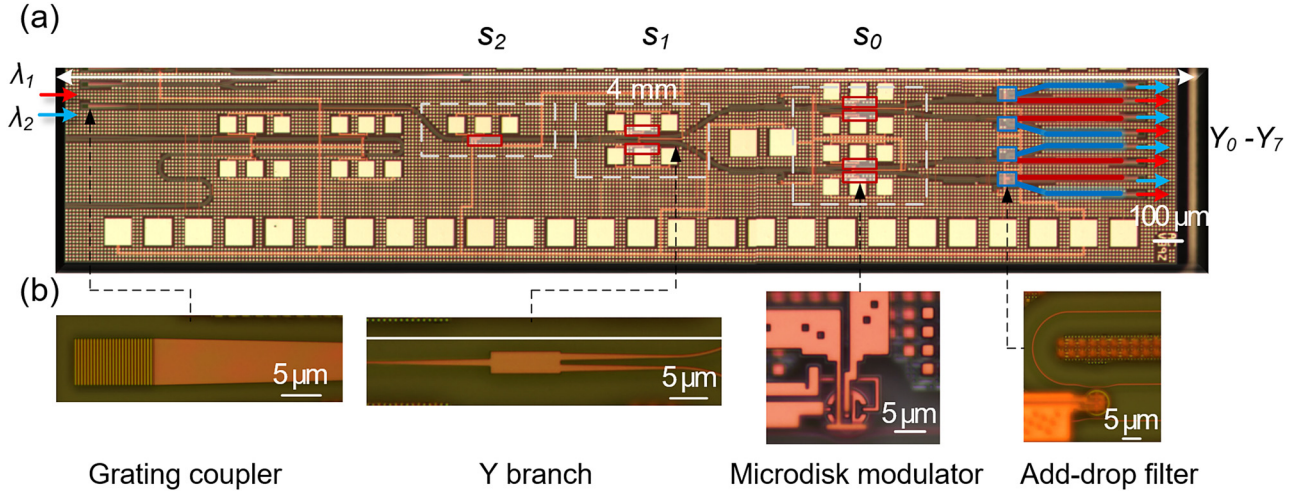


**Figure 2:** (a) Optical micrograph of the fabricated 3–8 line wavelength-division-multiplexing (WDM)-based electronic–photonic switching network (EPSN), the output ports for different wavelengths are shown in different colors. (b) Close-ups of some fundamental optical components such as grating coupler, Y branch (multimode interferometer), modulator, add-drop filter (demultiplexer/combiner).

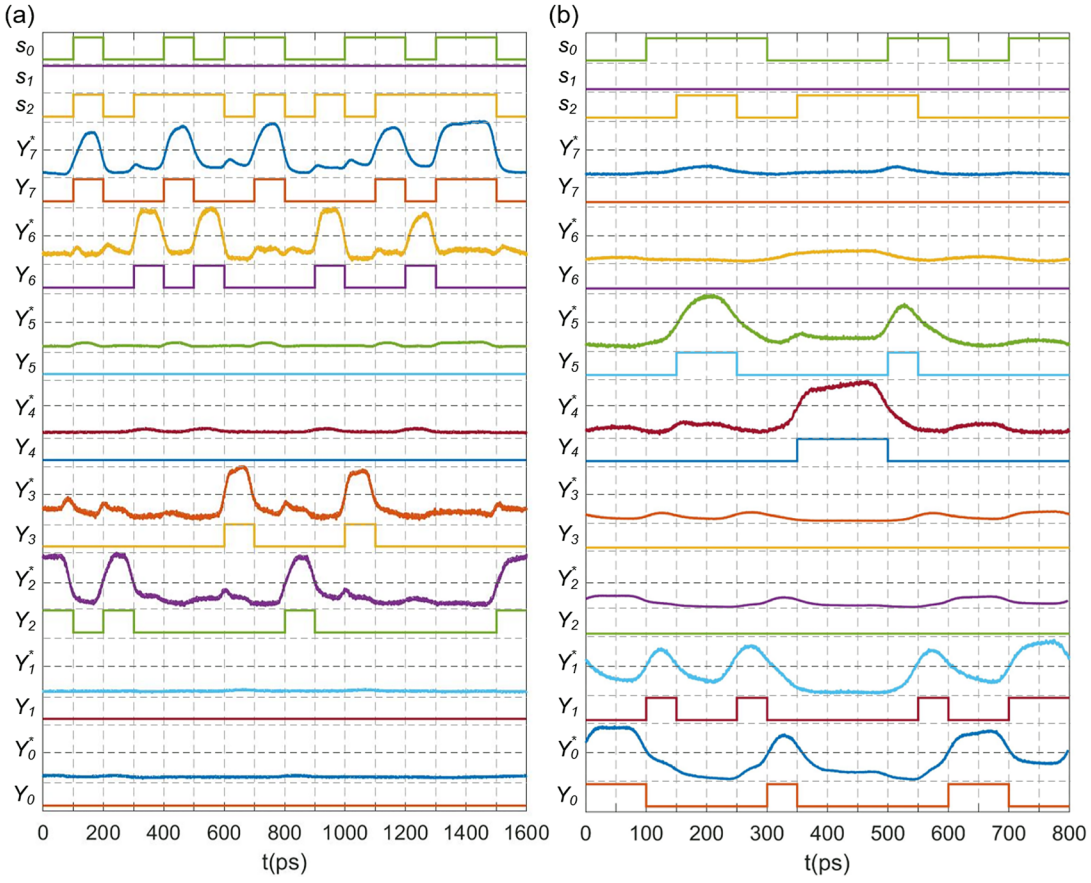


**Figure 3:** The logics of testing results of the decoder.
(a) The operating speed is 10 Gb/s. (b) The operating speed is 20 Gb/s. In this figure, $s_0$, $s_1$, $s_2$ are electrical input signals. The logics of output waveforms are shown as $Y_k$, while the original testing waveforms are shown as $Y^*_k$. The wavelength of $Y_0$–$Y_3$ is 1542 nm, while the operating wavelength of $Y_4$–$Y_7$ is 1566.8 nm. The logics of output waveforms are obtained by threshold detectors, and the threshold lines are shown in black dashed lines.

common in modern commercial CPUs [35]. To replace electrical counterparts, we should design the EPSN that is capable of operating on large bit numbers such as 16 (2 bytes) or 24 (3 bytes). In our cases, we can simply increase the size of the EPSN to achieve large bit number decoding/multiplexing. However, problems such as large propagation loss will emerge as too many optical logic gates, especially Y branches, are cascaded. Intending to reduce the propagation loss and other issues, we need to modify the design of the EPSN.

For simplicity, we will only discuss the optimization of the EPSN when it functions as an optical decoder in this section, while some specific designing approaches for EPMUX designs are also provided (see Supplementary S3). We suggest that an $N$–$2^N$ bit ($N = m + n$) decoder can be decomposed to $2^m$ sets of $n$–$2^n$ optical decoder units (ODUs). The optical components in ODUs are similar to those in Figure 1(c) except that $m$ cascaded modulators are added at the beginning of the network, which will function as an $m$-bit ENABLE (EN) gate. Each ODU, controlled by the EN gate, will generate the $2^n$ outputs independently. In this way, $3m$ dB propagation loss is reduced by reducing the number of Y branches. The overall power consumption of laser sources will remain unchanged, and $2^m$ CW input light beams are required in this architecture. It should be noted that the EO modulators for EN gates should be capable of modulating $\lambda_1$ and $\lambda_2$ at the same time. This requirement can be realized with broadband modulators or narrowband modulators whose resonant regions are carefully engineered.

One can also use cascaded ODUs and optical–electrical–optical (OEO) conversions to construct an $N$–$2^N$ bit ($N = m + n$) decoder. Shown in Figure 4(b), the first $m$ bits of the $N$-bit input signal are the inputs of an $m$-bit ODU where no EN gates are needed. The $2^m$ outputs of this $m$-bit ODU will then be the EN signal of the $2^m$ $n$-bit ODUs, which are

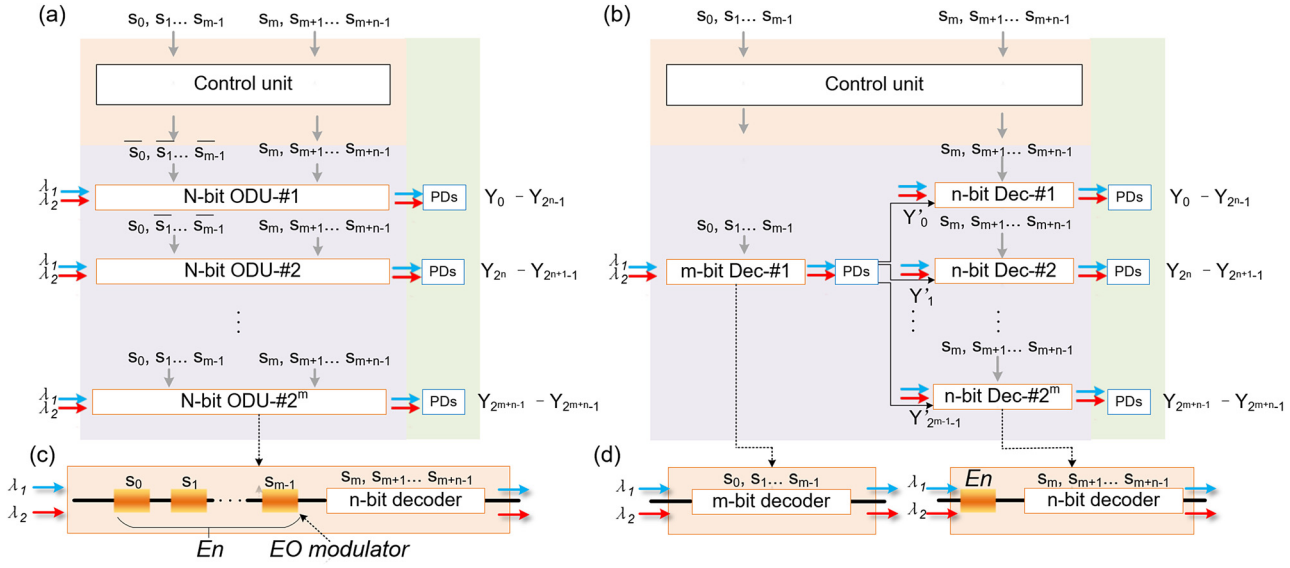


**Figure 4:** Schematic of the $N$–$2^N$ bit optical decoder.
It consists of a controlling unit to generate electrical inputs, optical decoder unit (ODU) arrays, and photodetector (PD) arrays. (a) Contains $2^m$ sets of $n$-bit ODUs controlled by $m$-bit ENABLE (EN) gates. (b) Contains one ODU to generate EN signals and $2^m$ sets of $n$-bit ODUs controlled by 1-bit EN gates. Schematics of the ODUs deployed in (a) and (b) are shown in (c) and (d), respectively.

controlled by 1-bit EN gates. The advantage of this structure is that it not only reduces $3m$ propagation loss but will also not introduce the insertion loss of cascaded modulators. What is more, the quality of the signal can also be improved during the OEO conversion. However, additional OEO conversions are required, which will increase the total latency of the $N$–$2^N$ decoder. Trade-offs between propagation loss and the latency should be made according to the value of $N$, which will be discussed hereinafter.

## 4.2 Delay

The proposed $N$–$2^N$ optical decoder utilizes light to transport information in the optical path in subpicoseconds, which is one or two magnitudes faster than electrical gates [36]. The time latency of an $N$-bit ($N = m + n$) decoder includes the EO time constant of the modulator $\tau_{eo}$, the latency of electrical signal $\tau_g$, the latency of each optical gate $\tau_o$, the optoelectronic transition time for PDs $\tau_{oe}$. The total latency can then be expressed as follows:

$$\tau = \tau_c + (m + n) \times \tau_o = \tau_c + N\tau_o \tag{1}$$

where $\tau_c = \tau_{eo} + \tau_g + \tau_{oe}$ is a constant. We assume $\tau_g$ for electronic gates is 7 ps in the state-of-the-art 7-nm technology [37], $\tau_{eo}$ and $\tau_{oe}$ for EO/OE conversion is 10 ps [32, 38], and $\tau_o$ is 0.3 ps [39]. It should be noted that $\tau_o = n_g L_{bit}/c$ is proportional to the length of the routing waveguide per bit $L_{bit}$, which can be optimized by advanced optical routing techniques. $n_g$ is the group index. Here, we calculate the operating speed of the optical decoder by assuming that the whole decoding procedure is expected to be finished in one clock cycle. The results shown in Figure 5 indicate that a 4-byte (32-$2^{32}$) optical decoder is capable of operating over 25 Gb/s and can go faster with the improvements of active components and passive components in the architecture.

The time latency of an $N$-bit ($N = m + n$) decoder based on cascading decoders can be written as follows:

$$\tau = \tau_c + (m + n + 1) \times \tau_o = \tau_{oe} + \tau_{eo} \tag{2}$$

where an additional OEO conversion will be required, which will slow down the operating speed. However, a 4-byte optical decoder using cascaded modulators can still be operated at around 20 Gb/s according to our calculation. It should be noted that OEO conversion has been largely reduced in recent years [40, 41]. The latency of the optical decoder can be further reduced with better OEO conversion techniques.

## 4.3 Loss

We define the propagation loss of each ODU as follows: $IL_{ODU} = P_{in}/P_{out}$, where $P_{in}$ is the power intensity of the input light beam and $P_{out}$ is that of the light beam at the selected output port. The propagation loss of the optical decoder is mainly contributed by the splitting loss of

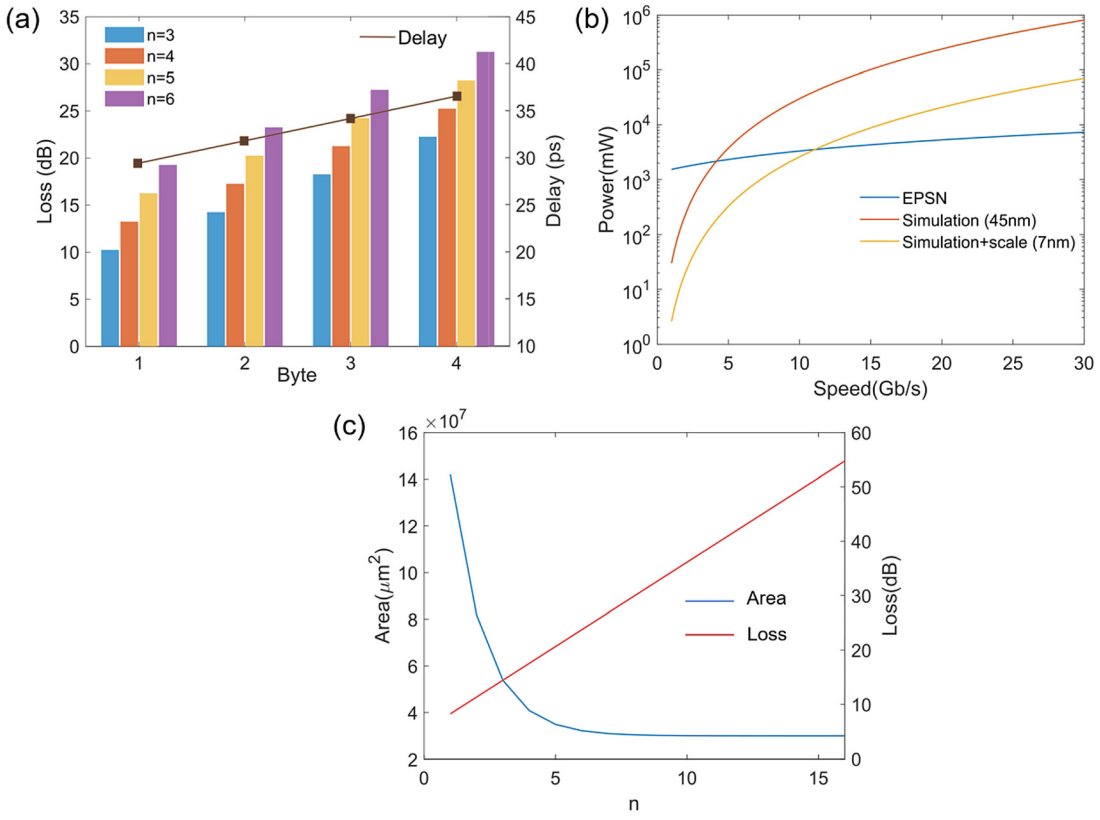


**Figure 5:** Performance analysis of the electronic–photonic switching network (EPSN).
(a) The propagation loss and the delay of an *N*-byte optical decoder with respect to the bit number of optical decoder units (ODUs) we use in the architecture. We use the architecture in Figure 4a in our design. (b) The power consumption estimation of a 16-$2^{16}$ EPSN in terms of operating speed, the performance of the electrical counterpart is also shown. (c) The trade-off between area and propagation loss of a 16-$2^{16}$ EPSN by choosing the value of *n*.

splitters, insertion loss (IL) of EO modulators, add-drop demultiplexers, and waveguides, which will accumulate in the optical critical path as the bit number of input signals increases.

Here, we evaluate the entire propagation loss of our EPSN by summing up the propagation loss of each optical component. The splitting loss caused by the Y branch in an $n$–$2^n$ ODU is $3(n-1)$ dB. The IL of each optical component includes IL of each modulator $\mathrm{IL_{Md}}$, the IL of each add-drop demultiplexer $\mathrm{IL_{DMUX}}$. Here, we neglect the propagation of optical waveguides and other passive waveguide structures, which can achieve less than 1 dB/cm on silicon photonic platform [34, 42]. The total propagation loss of an *N*-bit ODU can then be summarized as follows:

$$\mathrm{IL_{ODU}} = (3 + \mathrm{IL_{MMI}})(n-1) + (n+m)\mathrm{IL_{Md}} + \mathrm{IL_{DMUX}} \quad (3)$$

According to the Process Design Kit (PDK) document of current foundries [34], $\mathrm{IL_{MMI}}$ is 0.1 dB, $\mathrm{IL_{Md}}$ can reach 0.5 dB, $\mathrm{IL_{DMUX}}$ is 0.25 dB [34]. We can then evaluate the propagation loss for an $N$–$2^N$ decoder according to $m$, $n$ we select, which is shown in Figure 5(a). From Figure 5(a), we believe one can optimize the propagation loss of the decoder by reducing $n$. According to our footprint estimation, which will be discussed hereinafter, one need to make a trade-off between the propagation loss and the footprint of the EPSN by choosing $n$ to construct an $N$-bit EPSN ($N = m + n$).

For the architecture shown in Figure 4(b), there are two types of ODUs with different propagation loss according to $m$, $n$ we select. Using similar evaluation strategies, one can obtain the maximum propagation loss of these two ODUs:

$$\mathrm{IL_{ODU}} = (3 + \mathrm{IL_{MMI}})(\max(m,n) - 1) + (\max(m,n) + 1)\mathrm{IL_{Md}} + \mathrm{IL_{DMUX}} \quad (4)$$

## 4.4 Energy efficiency

The power consumption of the EPSN includes the power of the laser and the power consumption of EO modulators (electrical power). The laser power is determined by the total propagation loss of the EPSN, the sensitivity of

photodetectors, and the number of laser sources, while the electrical power is contributed by the power consumption of each EO modulator and the number of modulators. Therefore, one can use the following equation to estimate the total power consumption of the EPSN:

$$P_{\text{total}} = N_{\text{ODU}} \frac{P_{\min}}{\eta \text{IL}_{\text{ODU}}} + N_{md} P_{md} \tag{5}$$

where $N_{\text{ODU}}$ is the number of ODUs, $P_{\min}$ is the minimum detectable power of the photodetector, $\eta$ is the wall-plug efficiency of the laser, $N_{md}$ is the number of EO modulators, $P_{md}$ is the power consumption of each EO modulator. Figure 5(b) shows the curves of a 16-$2^{16}$ EPSN ($m = 0$, $n = 16$) in terms of operating speed based on our estimation.

The power consumption of a purely electrical 16-$2^{16}$ decoder based on 45- and 7-nm technology node is also shown in Figure 5(b) as a comparison. We first use commercial Synopsys Design Compiler (version 2017) to simulate the power consumption of the electrical decoder based on 45-nm technology node (gscl45nm). Then, the performance of the decoder in 7-nm technology node is calculated using scaling equations [37].

From Figure 5(b), one can infer that the merits of the EPSN begin to emerge when the operating speed is higher than 10 Gb/s. The power consumption of the EPSN can be about one order of magnitude smaller than the electrical counterpart when the clock rate exceeds 20 GHz. The advantages of using the EPSN for decoding will be expanded when it operates on a larger bit number since electrical circuits will suffer from severe interconnect issues as the number of transistors increases. Thanks to the achievements of integrated photonics, numerous energy efficient components have been presented and provided in current foundries. For instance, state-of-art EO modulators are capable of operating at 100 Gb/s while consuming only a few femtojoules per bit [14]. The power consumption of the EPSN can be further reduced if we deploy these energy-efficient components in our design. It should be noted that the thermal tuning power for aligning the resonant wavelength of each microresonator modulator is not included in Figure 5(b), while this part can be reduced or even eliminated with the development of photonic components. The detailed discussions of power consumption estimation are provided in Supplementary material S4.

## 4.5 Footprint estimation

As we know, optical computing units are usually larger than electrical counterparts since the basic building blocks, such as EO modulators and Y branches, are larger than transistors. Although the area of the optical computing module varies according to the placement and routing strategies, we try to characterize the scale of our EPSN by calculating the number of active components (EO modulators). For simplicity, we calculate the number of EO logic gates in an $N$–$2^N$ electronic–photonic decoder. The footprint of electrical circuits to control these EO logic gates is quite small compared to photonic circuits. Therefore, they will not be counted in area estimation.

We first discuss the architecture shown in Figure 4a. To an $N$–$2^N$ ($N = m + n$) decoder, the composed ODU can be treated as a conventional $n$-bit optical decoder controlled by an $m$-bit EN gate. In the EN gate, each bit requires one EO logic gate to control. The number of EO logic gates in a conventional $n$-bit optical decoder is $2^n$–1. Therefore, the total number of EO logic gates in an $N$–$2^N$ decoder is as follows:

$$N_{md} = 2^m \times (m + 2^n - 1) = (N - n - 1)2^{N-n} + 2^N \tag{6}$$

Similarly, one can obtain the architecture described in Figure 4(b) is as follows:

$$N_{md} = 2^m \times (1 + 2^n - 1) + 2^m - 1 = 2^{N-n} + 2^N - 1 \tag{7}$$

According to Eq. (1), choosing $m$, $n$ will not affect the total delay of the optical decoder but will determine the propagation loss of each ODU inferred from Eq. (3). The propagation loss of each ODU will reduce if we reduce the value of $n$. However, Eqs. S1 and S2 reveal a smaller $n$ leads to more EO logic gates. Figure 5(c) shows the trade-off between the propagation loss of each ODU and the estimated area of the 16-$2^{16}$ EPSN according to the $m$ and $n$ we choose. Here, we assume that each modulator/add-drop filter is $15 \times 17$ μm$^2$ and each Y branch is $50 \times 3$ μm$^2$ based on the PDK library files [34] and our measurement (Figure 2), while the area for optical routing is not considered for simplicity. From Figure 5(c), one should choose the combination of $m$ and $n$ and make trade-offs according to real scenarios. For example, when $m = 11$, $n = 5$, one can cooptimize the footprint and the propagation loss of each ODU.

As a comparison, an electrical decoder based on 7-nm technology node consumes about $1.14 \times 10^4$ μm$^2$ in area, which is more than 2600 times smaller than our proposed 16-$2^{16}$ EPSN. It is not surprising since even the smallest EO modulator or other optical component is still larger than transistors. However, the power density (the ratio between the power consumption and the area) of our EPSN will be about four orders of magnitude better than the electrical counterpart, which means our EPSN will not encounter overwhelming heat issues when operating at tens of Gb/s.

### 4.6 Performance optimization

As we have discussed, the proposed EPSN is capable of realizing high-speed and energy-efficient communications among modules or building blocks in the microprocessor. Actually, the performance metrics of our EPSN can be further enhanced in several directions.

Firstly, the propagation loss of the EPSN can be dramatically reduced by replacing the Y branch and the all-pass EO modulator with add-drop EO modulators. Add-drop EO modulators can achieve modulation by manipulating the flow of light and direct light to different optical paths. Therefore, an add-drop modulator can realize the functions of the modulator and the Y branch as well in our scenario. With add-drop modulators, we no longer need Y branches to split light to different ports, which will cause 3 dB splitting loss. Therefore, abandoning Y branches and using add-drop modulators can reduce the entire propagation loss of our EPSN. Furthermore, WDM can still be applied in our design since the add-drop modulator is a narrowband modulator.

Secondly, novel EO logic gates such as multioperand logic gates (MOLGs) can also be used in the design, leading to further reduction of the footprint, as well as the propagation loss of the decoder [43]. For example, an $m$-bit EN gate can be realized with one or two MOLGs, which will reduce the propagation loss without affecting the delay of our EPSN.

Thirdly, faster conversion time between electrical and optical signals will enhance the operating speed of the EPSN even further. From Eq. (4) and Figure 5, one can infer $\tau_{eo}$ and $\tau_{oe}$ contribute a constant time delay (20 ps), which dominates the computing speed of an EPSN, especially at low-bit data processing. With faster EO/OE conversion techniques, more electrical constituents can be replaced by optical circuits and more complicated optical data processing units can be designed.

Last but not least, our EPSN architecture can be optimized with VLSI designing strategies. For instance, instead of using an $N$–$2^N$ ($N = m + n$) binary decoder to control $2^N$ addresses, manipulating $2^N$ addresses can be achieved via a $m$–$2^m$ decoder and a $2^n$–$n$ multiplexer (see Supplementary material Fig. S1(b)). As a result, both the total number of EO logic gates and the propagation loss can be significantly reduced. A sample caption will be automatically inserted.

## 5 Conclusion

We have presented a novel EPSN that can realize the function of the binary decoder/multiplexer with an experimental demonstration at 20 Gb/s. Two wavelength–based WDM (1542 and 1566.8 nm in experiments) is exploited to reduce the number of modulators, scale down the size, and reduce the power consumption of the architecture. The performance of our architecture can be further improved with the development of modulators and OEO conversion techniques. Our architecture can be applied to accelerate the data transportation and processing between different units in the microprocessor.

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